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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,096	03/01/2004	Errol Todd Ryan	H1840	2466

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/791,096	RYAN ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,9-12,14-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,9-12,14-17,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Applicants' amendment to claim 2 has overcome the rejection made under 35 U.S.C. 112, second paragraph in the previous Office action. The rejection is therefore withdrawn.

Claim Rejections - 35 USC § 103

Claims 1, 2, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929).

Regarding claim 1, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59- column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10) within a thermal budget having a temperature dependent upon a silicide metal (the instant application on p. 9, lines 23-24 discloses that the thermal budget for nickel silicides is about 400 °C to 450 °C; Chang discloses forming the silicide at a temperature of about 400 to 800 °C, overlapping with the entirety of the thermal budget of nickel silicides).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes within the thermal budget for forming the silicide; and forming contacts in the contact

holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact holes within the thermal budget for forming the silicide (tungsten nitride, paragraph 0021; Lin discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 2, Chang and Lim together teach the method of claim 1. Lim further teaches that forming the contact liners uses an atomic layer deposition process (paragraph 0021).

Regarding claim 4, Chang and Lim together teach the method of claims 1 and 11. Chang further teaches that forming the silicide forms a nickel silicide (column 4, line 56 – column 5, line 10).

Regarding claim 5, Chang and Lim together teach the method of claim 1 and 11. Lim further teaches that forming the contacts forms a tungsten material (paragraph 0026); and forming the contact liners forms a tungsten nitride material (paragraph 0021).

Regarding claim 6, Chang teaches a method of forming an integrated circuit comprising providing a semiconductor substrate (**200** in Fig. 2D); forming a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); forming a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); forming source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and forming a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10) within a thermal budget having a temperature of less than about 400 degrees centigrade (Chang teaches forming the silicide at a temperature of about 400 °C to 800 °C, which overlaps with the claimed temperature range at about 400 °C, and since the claimed temperature range "less than about 400 degrees centigrade" is not specific, it could be interpreted as, for example, "less than 402 degrees centigrade," which Chang teaches).

Chang does not teach depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the

contact holes within the thermal budget for forming the nickel silicide; and forming tungsten contacts in the contact holes over the contact liners.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes (paragraph 0021) within the thermal budget for forming the silicide (Lin discloses keeping the reaction chamber at a temperature between 250 °C and 550 °C, a temperature range that overlaps with the thermal budget of nickel silicides); and forming tungsten contacts in the contact holes over the contact liners (paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Regarding claim 7, Chang and Lim together teach the method of claim 6. Lim further teaches that forming the tungsten nitride liners uses an atomic layer deposition process (paragraph 0021).

Claims 9, 11, 12, 15-17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as

applied to claims 6, 11, and 17 above, and further in view of Tseng (U.S. 2005/0035460).

Regarding claim 9, Chang and Lim together teach the method of claim 6 (note 35 U.S.C. 103(a) rejection above), but do not teach that forming the nickel silicide uses an ultra-thin thickness of a nickel silicide metal.

Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and taught by claim 6, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 11, Chang teaches an integrated circuit comprising a semiconductor substrate (**200** in Fig. 2D); a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; contact liners in the contact holes; and contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts. Chang also does not teach that the silicide is an ultra-thin silicide.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming contact liners in the contact holes; and forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of tungsten nitride and the contacts are formed of tungsten, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 12, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Chang further teaches that the silicide is a nickel silicide (column 4, line 56 – column 5, line 10).

Regarding claim 15, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts in the contact holes are tungsten (paragraph 0026).

Regarding claim 16, Chang, Lim, and Tseng together teach the integrated circuit as claimed in claim 11. Lim further teaches that the contacts are a tungsten material (paragraph 0026) and the contact liners are a tungsten nitride material (paragraph 0021).

Regarding claim 17, Chang teaches an integrated circuit comprising a semiconductor substrate (**200** in Fig. 2D); a gate dielectric on the semiconductor substrate (**206** in Fig. 2D; column 3, lines 36-39); a gate on the gate dielectric (**208** in Fig. 2D; column 3, lines 46-47); source/drain junctions in the semiconductor substrate (**210** in Fig. 2D; column 3, line 59-column 4, line 39); and a nickel silicide on the

source/drain junctions and on the gate (**234** in Fig. 2G; column 4, line 56 – column 5, line 10).

Chang does not teach an interlayer dielectric having contact holes therein above the semiconductor substrate; tungsten nitride contact liners in the contact holes; and tungsten contacts in the contact holes over the contact liners. Chang also does not teach that the silicide is an ultra-thin silicide.

Lim teaches depositing an interlayer dielectric having contact holes (paragraph 0020) therein above a semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners (tungsten, paragraph 0026).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Chang by additionally depositing an interlayer dielectric having contact holes therein above the semiconductor substrate; forming tungsten nitride contact liners in the contact holes; and forming tungsten contacts in the contact holes over the contact liners, as taught by Lim. The motivation for doing so at the time of the invention would have been that the method taught by Lim simplifies a deposition process of a tungsten nitride layer as a barrier metal, as expressly taught by Lim (paragraph 0014).

Additionally, Tseng teaches forming nickel silicide layers with a thickness of 50 – 350 Å (paragraph 0037), within the limits indicated in the instant specification on page 8, line 4 of "not more than 50 Å thickness."

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and further make the nickel silicide layer ultra-thin, as taught by Tseng. The motivation for doing so at the time of the invention would have been to provide a semiconductor device with reduced contact resistance, as taught by Tseng (paragraph 0009).

Regarding claim 20, Chang, Lim, and Tseng together teach the method of claim 17. Chang further teaches that the gate and source and drain regions are ion-implanted with arsenic prior to the formation of nickel silicide on the gate and source and drain regions, so the nickel silicide further comprises arsenic doping (column 4, lines 23-39).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) as applied to claims 6 above, and further in view of Tseng (U.S. 2005/0035460) and Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claim 10, Chang and Lim together teach the method of claim 6 (note 35 U.S.C. 103(a) rejections above), but do not teach that the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Tseng teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate an integrated circuit according to the method taught by Chang and Lim together, and taught by claim 6, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. 6,858,506) in view of Lim (U.S. 2004/0115929) and Tseng (U.S. 2005/0035460) as applied to claims 11 and 17 above, and further in view of Wolf et al. (*Silicon Processing for the VLSI Era*, Vol. 1).

Regarding claims 14 and 19, Chang, Lim, and Tseng together teach the device of claims 11 and 17 (note 35 U.S.C. 103(a) rejection above).

Tseng additionally teaches an interlayer dielectric made of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants (120 in Fig. 1; paragraph 0038).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate the integrated circuit taught by Chang, Lim, and Tseng together, and also taught by claims 11 and 17, and further make the interlayer dielectric of a material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants, as taught by Tseng. The motivation for

doing so at the time of the invention would have been to keep capacitance between metallization layers low, as taught by Wolf et al. (line 1 of Table 15.4, pg. 727).

Response to Arguments

Applicant's arguments filed 10/11/2005 have been fully considered but they are not persuasive.

Applicant argues on pages 8 and 10 that "Chang is silent with respect to a 'thermal budget having a temperature dependent upon the silicide metal,' and therefore teaches away from Applicants' invention as claimed." This argument is not persuasive because, as pointed out in the rejection of claim 1 above, Chang teaches forming the silicide at a temperature of about 400 to 800 °C, which includes the range 400 to 450 °C, which Applicant discloses is the thermal budget for nickel silicide.

It has been held that "in the case where the claimed ranges 'overlap or lie inside ranges disclosed by the prior Art' a prima facie case of obviousness exists." *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); *In re Geisler*, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of "50 to 100 Angstroms" considered prima facie obvious in view of prior art reference teaching that "for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms]." The court stated that "by stating that suitable

protection' is provided if the protective layer is about' 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant's] claimed range.").

Chang may be silent regarding the motivation for forming the silicide within a particular temperature range, but does teach using a temperature within the range disclosed by Applicant to be within the thermal budget for nickel silicide.

Likewise, contrary to Applicant's argument on pages 9 and 11 that since Lim is silent regarding the formation of any silicide, much less within the thermal budget claimed by Applicants, Lim fails to teach or suggest Applicants' invention as claimed in claim 1, Lim teaches forming a contact hole liner of tungsten nitride at a temperature of 250 °C to 550 °C, encompassing the thermal budget that Applicant discloses as relevant to nickel silicide. Lim does teach forming the contact liner at a temperature that is compatible with nickel silicide, as defined by Applicant—it is not necessary for Lim to have the same reason disclosed by Applicant to do so.

Applicant further argues on page 9 that Chang and Lim teach away from each other. However, this is not the case. Lim may not expressly recognize the problem of forming contact liners in semiconductors having silicide layers, but Lim does teach forming the contact liners within a temperature range disclosed by Applicant to be compatible with the nickel silicide layer taught by Chang.

Finally, on page 14, Applicant argues that since Tseng teaches forming a silicide layer between 50 and 350 Å, Tseng teaches away from Applicant's claimed "ultra-thin" silicide layer, disclosed to have a thickness "not greater than 50 Å." However, "not greater than 50 Å" includes 50 Å, which Tseng teaches.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

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